8 (amended). An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed centrally on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate [adhered to said second surface of said substrate]; and

wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips.

In claim 15, lines 1-2, replace "claim 6" which - - claim 8 - -.

16 (amended). An integrated circuit package comprising:

a substrate having a plurality of peripheral openings, first and second surfaces and an outline;

a plurality of routing strips being integral with said substrate;

a plurality of pads centrally disposed on said first surface at least one of said pads being electrically connected with said routing strips;

a chip adhered to said second surface of said substrate, said chip having an outline that is substantially the same as said outline of said substrate and having a plurality of bonding pads located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate;

wire bonding electrically connecting said bonding pads to said routing strips;

vias connecting said routing strips to said pads;

potting material filling said peripheral openings and covering said wire bonding and said bonding pads; and

a plurality of solder balls centrally disposed on said pads disposed on said first surface of said substrate forming a high density ball grid array.

Please replace pending claim 8 with the following claim having the same number, and replacement claim 8 is also shown in re-written form, with underlining showing additions, on a sheet attached to this Amendment and filed herewith:

9 ~~8~~ (twice amended). An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed centrally on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads physically attached to the chip and located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate; and

wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips.

Please replace pending claim 11 with the following claim having the same number, and replacement claim 11 is also shown in re-written form, with underlining showing additions, on a sheet attached to this Amendment and filed herewith:

12 ~~11~~ (amended). The integrated circuit package as recited in claim 9 ~~8~~ further comprising a plurality of solder balls disposed on said pads.

Rejections Under 35 U.S.C. § 112, second paragraph

Claim 2 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The Examiner states:

> Claim 2 recites the limitation "said substrate has a first and second layer" in line 12, page 29. There is insufficient antecedent basis for this limitation in the claim. Rather, the specification, page 20, line 10 describes "Figure 2 depicts printed circuit board 70 as having two layers, top layer 76 and bottom layer 78, it should be understood by one skilled in the art that printed circuit board 70 may consist of a single layer or may be a multilayered board." Applicant must modify either the specification or claim 2 acknowledging that the printed circuit is multilayer or it is a single layer.

Applicants respectfully request reconsideration of this rejection and submit that no amendment to claim is statutorily required. Claim 2 currently recites:

> 2. The integrated circuit package as recited in claim 1 wherein said substrate has a first and a second layer.

The Specification provides unambiguous support for claim 2. For example, the Specification states, at page 14, lines 4-5:

> The printed circuit board 70 depicted has two layers, a top layer 76 and a bottom layer 78.

Thus, it is respectfully submitted that claim 2 complies with 35 U.S.C. § 112, second paragraph. In addition, Applicants respectfully submit that there is no legal basis to require them to "modify either the specification or claim 2 acknowledging that the printed circuit is multilayer or it is a single layer." Instead, the text quoted above by the Examiner pertains to alternative embodiments, and it is clearly within the right of an applicant to set forth alternatives in its specification. Thus, in the present application, various alternatives are provided, including in one such alternative implementing circuit board 70 from a "single layer" whereas in other embodiments circuit board 70 is formed from more than one layer (i.e., it is "multilayered").

Rejections Under 35 U.S.C. § 103(a)

Claims 1 through 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi (US Patent 5,886,876). Claim 1 is now amended such that an additional limitation is added to the claim, namely, that the claimed integrated circuit package include:

> a plurality of electrical conductors coupled to said chip and located such that each electrical conductor in said plurality of electrical conductors is aligned within a respective one of said plurality of peripheral openings in said substrate

Antecedent support for the claim language is located in the Specification in various locations such as at page 12 and also may be observed with respect to Figure 1, wherein it is shown that printed circuit board 70 includes openings (86) and within those openings are bonding pads (120). Applicants respectfully submit that Yamaguchi US Patent 5,886,876 does not show, teach, or suggest this amendment in combination with the remaining recitations in claim 1. Accordingly, claim 1 and its dependent claims 2 through 7 and 21 are in condition for allowance.

Independent claim 8 also has been amended with language comparable in various respects to the amendment to claim 1. Specifically, claim 8 previously recited a "a chip having a plurality of bonding pads," and that claim is now amended to recite that those pads are:

> located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate

Applicants respectfully submit that Yamaguchi US Patent 5,886,876 does not show, teach, or suggest this amendment in combination with the remaining recitations in claim 8. Accordingly, claim 8 and its dependent claims 9 through 15 are in condition for allowance.

Independent claim 16 also has been amended with language comparable in various respects to the amendment to claim 1. Specifically, claim 16 previously recited a "a chip . . . having a plurality of bonding pads," and that claim is now amended to recite that those pads are:

> located such that each bonding pad in said plurality of bonding pads is aligned within a respective one of said plurality of peripheral openings in said substrate

Applicants respectfully submit that Yamaguchi US Patent 5,886,876 does not show, teach, or suggest this amendment in combination with the remaining recitations in claim 16. Accordingly, claim 16 and its dependent claims 17 through 20 are in condition for allowance.

New Claims

New dependent claim 21 and new independent claim 22 are added, and it is respectfully submitted that no new matter is introduced by these claims. New claim 21 depends from an allowable claim (i.e., claim 1) and, hence, it is respectfully submitted that claim 21 is in condition for allowance. Finally, new independent claim 22 is added. The language from claim 22 is comparable in various respects to other pending claims, with an alternative recitation including "a chip comprising an operative side and a non-operative side, wherein said chip is adhered to said second surface of said substrate such that the non-operative side faces away from the substrate." Antecedent support for this language may be found in the Specification at page 27, lines 7-10 which state:

> The potting and encapsulation of the integrated circuit package 30 of the present invention as described herein also reduces the overall profile by allowing the non-operative or backside of the silicon chip 50 to be exposed.

Applicants respectfully submit that this new claim 22 is also patentable over the art of record.

Fees

The present Amendment adds one dependent and one independent claim, thereby bringing the total claims submitted for this application equal to 22 and with a total of four independent claims, with Applicants having previously paid for three independent claims. Thus, the additional fees of $116.000, for claims over 20 (2*$18=$36) and the single independent claim in excess of three ($80), are respectfully requested to be charged to deposit account number 20-0668 of Texas Instruments Incorporated as indicated in the Fee Transmittal (for FY 2001) sheet filed herewith.

fi

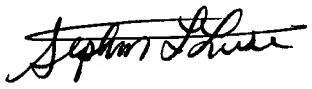
The fee for the enclosed petition for an extension of time for a one (1) month extension is also addressed in the Fee Transmittal (for FY 2001) sheet filed herewith.

The Commissioner is also hereby requested and authorized to charge charge any additional fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Conclusion

From the above, Applicants respectfully submit that all of the pending claims in this case are patentably distinct in view of the record in this case. Entry of the above amendment in, and reconsideration of, the above-referenced application are respectfully requested.

Respectfully submitted,



Stephen L. Levine
Registry No. 33,413
Attorney for Applicant

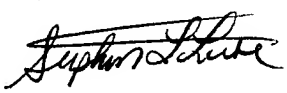
Anderson, Levine & Lintel, L.L.P.
12160 Abrams Road, Suite 111
Dallas, Texas 75243
(972) 664-9552

CERTIFICATE OF MAILING
37 C.F.R. § 1.8

The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Commissioner for Patents
Washington, DC 20231

on **January 16, 2001.**



Stephen L. Levine
Registry No. 33,413